Pseudo Asynchronous Level Crossing ADC for ECG Signal Acquisition

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Abstract—A new pseudo asynchronous level crossing analogue-to-digital converter (ADC) architecture targeted for low-power, implantable, long-term biomedical sensing applications is presented. In contrast to most of the existing asynchronous level crossing ADC designs, the proposed design has no digital-to-analogue converter (DAC) and no continuous time comparators. Instead, the proposed architecture uses an analogue memory cell and dynamic comparators. The architecture retains the signal activity dependent sampling operation by generating events only when the input signal is changing. The architecture offers the advantages of smaller chip area, energy saving and fewer analogue system components. Besides lower energy consumption the use of dynamic comparators results in a more robust performance in noise conditions. Moreover, dynamic comparators make interfacing the asynchronous level crossing system to synchronous processing blocks simpler. The proposed ADC was implemented in 0.35μm complementary metal-oxide-semiconductor (CMOS) technology, the hardware occupies a chip area of 0.0372 mm$^2$ and operates from a supply voltage of 1.8 V to 2.4 V. The ADC’s power consumption is as low as 0.6 μW with signal bandwidth from 0.05 Hz to 1 kHz and achieves an equivalent number of bits (ENOB) of up to 8 bits.

Index Terms—Analogue-to-digital conversion (ADC), Asynchronous Level Crossing ADC, ECG recording, Level crossing ADC, Level crossing sampling, Analogue memory cell, Dynamic comparator.

I. INTRODUCTION

This continuous push for smaller and more energy efficient systems necessitates the development of new signal acquisition methods. In the search for more efficient signal acquisition methods, it has been established that for capturing many types of bio-medical signals, asynchronous level crossing ADCs offer low power and low mean data rate advantages compared to their uniform time interval sampling counterparts [1], [2]. These advantages are achieved, since, most of these signals are sparse in the time domain [1], [2].

Even though, the data reduction and low power advantages of the asynchronous level crossing ADCs are well established [2], [3], [4], [5], asynchronous level crossing ADCs usage is still limited partly due to the difficulty of interfacing the ADCs to synchronous systems, which form the bulk of digital systems. Moreover, due to the continuous time operation of most existing asynchronous ADCs, interfacing to switched capacitor systems would also be challenging. Thus, we propose a new architecture of a level crossing ADC that is simpler to interface with synchronous systems. Furthermore, the architecture retains the signal dependent operation advantage of level crossing ADCs, while reducing chip area and power consumption.

We herein present a pseudo asynchronous ADC architecture that is predominately digital. Our proposed architecture builds upon the work of others, who contributed several ideas to shape what we know today as the state-of-the-art in asynchronous ADC design. These contributions range from putting forward the concepts [6], [7], [8], to various architectures and associated improvements [1], [9], [10], to methods for asynchronous signal processing [11], [12], to proposing new design approaches that yield different advantages like reducing the amount of data and energy used [1], [2], [3], [4], [5]. There have been numerous contributions aimed at the improvement of the energy efficiency of the asynchronous ADCs. These works have made valuable contributions along the lines of low voltage powered asynchronous ADC designs with low resolution, more energy efficient DAC architectures [2], [5] and in some cases even replacing the DAC with an integrator circuit [10].

We propose an approach that not only reduces energy, but also makes the ADC more noise robust and simpler to interface with synchronous systems. The proposed asynchronous level crossing ADC architecture also reduces/simplifies the analogue parts of the ADC. Moreover, the reduction of analogue components fits in very well with sub-micron technologies [2], [10]. We eliminate the typical continuous time comparators and DAC found in most asynchronous ADC architectures [1], [2], [13] and replace these with dynamic comparators and an analogue memory cell respectively [14], [15], [16], [17]. The use of dynamic comparators means that our comparators are not continuously drawing power, thus lowering power consumption. Additionally, dynamic comparators make our ADC simpler to interface with synchronous systems. Furthermore, we do not capture the actual voltage values in digital form and then convert them to analogue form by a DAC to feedback as it is done in most of the asynchronous/level crossing ADC architectures thus far presented [1], [2], [5], [9].

These changes simplify the circuitry and improve the ADC’s performance in terms of chip area usage, power consumption and noise robustness. Besides these advantages, the reduction
of analogue parts makes the architecture better supported by sub-micron semiconductor processes. In this paper we explain the development of the proposed ADC architecture. Section II presents the proposed architecture including the derivation of an SNR formula for the proposed ADC architecture. In Section III, we present the CMOS implementation of the proposed ADC architecture. Section IV presents the performance analysis and hardware verification. In Section V we compare our proposed architecture with other works and discuss the architecture’s advantages, disadvantages and possible improvements for the implementation. We draw conclusions in Section VI.

II. PSEUDO ASYNCHRONOUS ADC ARCHITECTURE

We propose a new asynchronous level crossing ADC architecture that reduces and simplifies the analogue parts of the ADC. We achieve this by eliminating the typical continuous time comparators and DAC found in most asynchronous level crossing ADC architectures [1], [2], [3], [9] and replace these with dynamic comparators [18], [19], [20] and an analogue memory cell [14], [15], [16], [17] respectively. The term pseudo in the title comes from the fact that the comparators are clocked. Replacing of the continuous time comparator with clocked dynamic comparators changes the way the ADC works. Besides the changes in the hardware architecture, we also propose a simple data encoding method for the proposed ADC.

A. Typical Asynchronous ADC Architecture

We begin by examining the typical asynchronous level crossing ADC architecture as depicted by [1]. This architecture is classified as the floating window architecture [10]. Figure 1 shows a block diagram of a common level crossing ADC architecture. In the figure the DAC holds the last level crossed, while the comparators CM1 and CM2 check for up and down signal level crossing events, respectively. The control logic block is an asynchronous control logic block whose state machine is driven by pairs of request (REQ) and acknowledge (ACK) handshake lines as opposed to a synchronous clock [9]. The most common general formula for calculating SNR for asynchronous ADC’s was derived in Sayiner’s work [13]. In the derivation the SNR of the ADCs was given by:

\[
\text{SNR} = 20 \log(R) - 11.2 \text{ (dB)} \quad (1)
\]

where \( R \) is the ratio of the counter frequency to the input signal frequency assuming a sinusoidal input signal. The expression in Equation 1 is obtained by applying the Riemann integral (integration on the time interval). However, there was a suggestion by [21], that this derivation should be done via Lebesgue integration which is more suited to level crossing ADCs. Riemann integration results is a 3dB overstatement of the SNR. The corrected expression is given in Equation 2:

\[
\text{SNR} = 20 \log\left( \frac{3 \cdot P(V_{in})}{P(dV_{in}/dt) \cdot T_C} \right) \text{ (dB)} \quad (2)
\]

Both of these equations are based on ideal error free DACs, thus they only consider the error due to time quantization. The SNR equation derivation method in [9] is similar to that in [13]. However, the derivation in [13] is simplified by assuming a pure sinusoidal signal, while that in [9] is left in a form that takes into account the spectral components of the signal.

\[
\text{SNR} = 10 \log\left( \frac{3 \cdot P(V_{in})}{P(dV_{in}/dt) \cdot T_C} \right) \text{ (dB)} \quad (3)
\]

where \( V_{in} \) is the input voltage, \( T_C \) is the timer period and \( P(x) \) is the power of component \( x \).

B. Proposed Asynchronous ADC Architecture

Level crossing ADCs based on the block diagram in Figure 1 have been implemented [1], [2], [9]. The challenges with the architecture in relation to our application are:

- High energy consumption of the DAC and comparators [1].
- High area requirement of energy efficient DAC architectures which work at low frequencies.
- Difficulty in interfacing purely asynchronous level crossing ADCs to low power, small chip area clocked systems with no buffering memory.

The main goals of our architecture are reducing the amount of data generated, chip area usage, energy consumption, and improve noise robustness as well as simplify interfacing to synchronous digital and switched capacitor circuits. To achieve our goals we depart from the existing architecture by:

- Not capturing digital voltage levels, but just timer values and event flags.
- Replacing the DAC with an analogue memory cell.
- Replacing the continuous time comparators with differential dynamic comparators.
- Developing a compact state machine and data path to respond to signal events and control the ADC.

By not capturing digital voltage levels but timer values and event flags, we are able to reduce the mean data rate. The elimination of the DAC block from the signal path also eliminates the need to digitize the level crossing value and store it in digital form, so that it can be converted back to analogue form and fed back to the differential amplifiers [8], [9], [11], [13]. Eliminating the DAC also eliminates the voltage counter and associated logic. The use of dynamic comparators reduces power consumption and chip area. Moreover, dynamic comparators make our ADC more robust to noise and simpler to interface with synchronous systems and switched capacitor...
circuits. These actions combined, simplify the implementation and reduce the power consumption of the ADC. Figure 2 shows the proposed architecture of the asynchronous level crossing ADC. The proposed architecture uses differential comparators which eliminates the need for difference amplifiers. Figure 3 shows the timing diagram of the proposed ADC. The asynchronous controller is driven by the state of the dynamic comparator outputs. Indeed, the ENC signal and the dynamic comparator output signals are used as asynchronous handshake signals. The ENC signal acts as the request signal while the dynamic comparator outputs are also the acknowledge signals. The converter output DOUT is determined by three sources of events which are, signal up level crossing event from dynamic comparator DCU, signal down level crossing event from dynamic comparator DCD, and the overflow event of the timer. When any of the said events occur, the timer value is captured and encoded appropriately to give DOUT. In the case of a timer overflow event, only a flag of the overflow event is recorded for time keeping purposes. More details of the operation and a state machine for the asynchronous ADC controller are provided in Section III.

C. ADC Design Parameters

The proposed architecture introduces changes to the floating window asynchronous level crossing ADC architecture. These changes made to the floating window asynchronous level crossing ADC design necessitate the development of an approach of selecting system parameters.

1) Clocked Comparators and the Bernstein Criterion: We have replaced the continuous time comparators with dynamic comparators, therefore we need to ensure that the dynamic comparators are scanned at a rate that is fast enough for the input signal. For this we use the Bernstein criterion, the use of this criterion was proposed by [9]. This criterion gives us the minimum scan frequency for our dynamic comparators and is also used to determine the maximum allowable update time for the analog memory cell. We derive the scan period \( \tau \) as follows: Let \( V_{in} \) be a band limited input signal with band width \( B \) given by \( f_1 \leq B \leq f_u \). We consider the highest frequency component in the signal; \( f_u \) as a sinusoidal component such that

\[
V_{in} = A \cdot \sin(2\pi f_u t)
\]

where \( A \) is the signal amplitude and \( f_u \) is the signal frequency and \( t \) is the time. The slopes in the signal are given by the derivative of the signal. The derivative of the signal is given by:

\[
\frac{dV_{in}}{dt} = A \cdot 2\pi f_u \cdot \cos(2\pi f_u t).
\]

The fastest slope in the signal occurs at

\[
\frac{dV_{in}}{dt} = A \cdot 2\pi f_u.
\]

To ensure that the dynamic comparators scan the time axis fast enough, we should as a minimum condition make sure that the scan period \( \tau \) is less than or equal to the time it takes the signal to change by a single threshold \( \Delta V \). From the derivative this means that

\[
\frac{\Delta V}{\tau} \geq A \cdot 2\pi f_u.
\]

Thus the scan period is given by:

\[
\tau \leq \frac{\Delta V}{A \cdot 2\pi f_u}
\]

but \( 2 \cdot A/\Delta V = 2^N \) where \( N \) is the resolution of the level crossing step in bits. For our design \( N \) is also the memory cell resolution, we will refer to \( N \) as the corresponding \( \Delta V \) resolution or memory cell resolution. The scan frequency \( f_s \) is therefore given by:

\[
f_s \geq \frac{2^N \cdot \pi \cdot f_u}{4}.
\]

Equation 9 is the Bernstein criterion that should be satisfied for our proposed architecture. We note that for most applications it is not usual for the input signal to make a full-scale change at its maximum frequency [1]. However, since ECG signals are low frequency signals, this apparent overstating the scan frequency has a low penalty on energy consumption. Furthermore, designing for extreme cases is good practice, especially for noisy environments. Figure 4 shows results from a Monte-Carlo simulation of a model of our proposed ADC.
while sweeping the input frequency. We observe that there is a sharp degradation of reconstructed signal’s SNR as soon as the input frequency passes the Bernstein criterion input frequency limit. Within the Bernstein criterion input frequency limit, we note there is little to no benefit in increasing the scan frequency. The gray area shows the 95% confidence interval of the SNR. We notice that the SNR variance is higher for lower ∆V resolutions, as expected. Furthermore, the fall in SNR for higher frequencies is advantageous, since it also means that our ADC would naturally attenuate out-of-band noise, thus contributing to a more robust performance compared to typical level crossing ADCs.

2) Analogue Memory Cell Resolution and Hold Time: The analogue memory cell replaces the DAC. The function of the analogue memory cell is to hold the last voltage level crossed. Thus, the memory cell’s resolution is analogous to the DAC’s resolution. However, unlike most DACs, the analogue memory cell is volatile and has a finite storage/hold time. It is desirable to have long memory cell storage times since this reduces the impact of the leakages on the performance of the ADC at the lower cutoff frequency of the signal. As such the hold time is important for deciding the lower frequency cutoff of the ADC. Let \( f_l \) be the lower cutoff frequency and \( N \) bits be the memory cell resolution, while \( T_{H_{min}} \) is the minimum required hold time. The relationship between the lower cut-off frequency \( f_l \) and the minimum hold time \( T_{H_{min}} \) also defines the maximum allowable signal change time \( \Delta T_{max} = T_{H_{min}} \) for our system. For a sinusoidal signal at the lower cutoff frequency of \( B \), the slowest rates of change occur close to the turning points. At the worst case turning point the signal gets infinitesimally close to the threshold level, but does not cross the threshold. Figure 5 shows the worst case turning point. Therefore, the minimum memory cell hold time required for

\[
\Delta T \approx \Delta V \left( \frac{dV_{in}}{dt} \right)^{-1}
\]

Furthermore, consider a memory cell with a reasonably flat hold time (leakage) profile such as shown in Figure 19, with a mean hold time of \( T_{H} \) at \( \Delta V \) corresponding to resolution \( N \) bits. The error contributed by the finite hold time of the memory cell is:

\[
\epsilon V_m = \Delta T / T_{H} \cdot 2^N \cdot \frac{A}{2^N} = \left( \frac{dV_{in}}{dt} \right)^{-1} \cdot \frac{4 \cdot A^2}{T_{H} \cdot 2^{2N}} \tag{12}
\]

If we consider the case where \( V_{in} \) is a pure sinusoidal signal, then we get

\[
\epsilon V_m = (A \cdot 2\pi f \cdot \cos(2\pi ft))^{-1} \cdot \frac{4 \cdot A^2}{T_{H} \cdot 2^{2N}} \tag{13}
\]

\[
\epsilon V_m = \sec(2\pi ft) \cdot \frac{4 \cdot A}{2\pi f \cdot T_{H} \cdot 2^{2N}} \tag{14}
\]

To find the power of \( \epsilon V_m \) we apply Lebesgue integration (along the vertical axis):

\[
P(\epsilon V_m) = \frac{2}{\pi} \left[ \frac{2 \cdot A}{\pi f \cdot T_{H} \cdot 2^{2N}} \right]^2 \tag{15}
\]

\[
\frac{2^N}{2A} \int \left( \sec \left( \arcsin \left( \frac{x}{A} \right) \right) \right)^2 dx
\]
\[ P(\varepsilon V_m) = \left( \frac{2 \cdot A}{\pi^2 \cdot T_H \cdot 2^{2N}} \right)^2 \]

Equation 16 shows the error contributed by the memory cell leakage. As the corresponding resolution of \( \Delta V \), \( N \) bits, is increased, the natural logarithm term approaches zero, such that the impact of the memory cell leakage on the total error is reduced. However, due to the increase in precision requirements, the achievable memory cell hold time (\( T_H \)) is also reduced. Therefore, we need to make a trade-off between the resolution \( N \), and the hold time \( T_H \). The error due to time quantization is given by:

\[ \varepsilon V_q = \frac{dV_{in}}{dt} \cdot \delta t \]

where \( \delta t \) is a uniformly distributed random variable in \([0, T_C]\). From [21], \( \varepsilon V_q \) is given by:

\[ P(\varepsilon V_q) = \frac{1}{2A} \int_{-A}^{A} \left( A \cdot 2\pi f \cdot \cos \left( \arcsin \left( \frac{x}{A} \right) \right) \right)^2 dx \]

The total error power is given by:

\[ P(\varepsilon) = P(\varepsilon V_q) + P(\varepsilon V_m) \]

Equation 22, gives the SNR for our architecture.

\[ SNR = 10 \log \left( \frac{P(V_{in})}{P(\varepsilon V_q)} \right) \]

Where \( P(V_{in}) \) is also obtained by Lebesgue integration according to [21].

\[ P(V_{in}) = \frac{1}{2A} \int_{-A}^{A} \left( A \cdot \sin \left( \arcsin \left( \frac{x}{A} \right) \right) \right)^2 dx = \frac{A^2}{3} \]

Then the SNR Equation becomes

\[ SNR = 10 \log \left( \frac{3\pi^2 \cdot 2^{3N} \cdot T_H^2 f^2}{2^{4N+3} \cdot \pi^4 f^4 \cdot T_C^2 \cdot T_H^2 + 9 \ln \left( 1 + 2^{-N} \right)} \right) \]

We let \( R_C = T_C \cdot f \) and \( R_H = T_H \cdot f \), Equation 24 becomes:

\[ SNR = 10 \log \left( \frac{3 \cdot \pi^2 \cdot 2^{3N} \cdot R_C^2 \cdot R_H^2 + 9 \ln \left( 1 + 2^{-N} \right)}{2^{4N+3} \cdot \pi^4 R_C^2 \cdot R_H^2 + 9 \ln \left( 1 + 2^{-N} \right)} \right) \]

Just as it is in the floating window level crossing architecture, Equation 25 shows that the SNR variation for the ADC is still dominated by the relationship between the signal frequency and the clock frequency [13]. This is expected since the \( R_C \) variable is the inverse of the ratio \( R \) in Equation 1. For the asynchronous level crossing ADC with an ideal DAC the SNR is constant for each \( R_C \) value [13]. Figure 6 shows the relationship between the SNR at different values of \( \Delta V \), the memory cell hold time \( T_H \) and the \( R_C \) variable. The \( T_H \) has a uniform distribution with standard deviation of 5%. As \( R_C \) gets larger, there is a fall in SNR values. This is expected since large values of \( R_C \) mean that we are reducing our clock/timer frequency relative to the signal frequency. Furthermore, we notice that the memory cell hold time only affects SNR at the lowest value of \( R_C \), which corresponds to a low input frequency of 0.05 Hz. This is because lower values of \( R_C \) occur at low signal frequencies, where the memory cell hold time is influential. As expected from Equation 25, we see in Figure 6 that as the \( \Delta V \) resolution is increased, the performance at most of the \( R_C \) values is only slightly improved. However, for the line \( R_C = 1.5 \cdot 10^{-6} \) there is great variation in performance with changes in both \( T_H \) and \( \Delta V \) resolution. This is due to the impact of the memory cell leakage at the low input signal frequency of 0.05 Hz, which is modified by both changes in \( \Delta V \) resolution and \( T_H \). As \( T_H \) is increased, the performance at the low value of \( R_C \) improves. Likewise, as the \( \Delta V \) resolution is increased, the performance of the low \( R_C \) line also improves because of the increase in events, which results in reduced dependency on memory cell hold time.

III. IMPLEMENTATION

A. Analogue Memory Cell

Analogue memory cells have been developed as parts in neural networks and various adaptive circuits where high density analogue data storage is required in real-time [22],
The ADC architecture being presented makes use of a low power volatile analogue memory cell. We had various options of implementing analogue memory cells, some of which are [14], [15], [17], [24]. Moreover, floating gate technology memory cells are also known to offer long term storage. However, they are not suitable due their high voltage write requirements and long write times and non-volatility [25], [26]. Our main objectives with regards to the analogue memory cell were:

- Short to medium term storage time.
- Fast update time to minimize control loop delays [27].
- Low power consumption and small chip area usage.

The storage time requirement may be achieved by the use of ultra low leakage switch structures as presented in [17], [25], [28]. However, these switch architectures have a drawback of being unidirectional, thus limiting the memory cell update speed. To achieve the objectives listed above, we chose a memory cell design based on leakage current compensation [29]. A top level schematic showing the basic structure of the analogue memory cell is shown in Figure 7. All switches are complementary gates of length and width 1.2 µm and 1 µm respectively. The load capacitor (C_L) is 40 pF and the dummy capacitor (C_D) is 250 fF, they are both Poly-Poly capacitors. The load capacitor’s size is a trade-off between the hold time, the area occupied and the need to minimize effects of charge feed through on the load capacitor [30]. The leakage current compensation technique applied in the memory cell architecture is based on a leakage current compensation technique presented in [29]. We made a few improvements on the design in [29] by introducing a cascaded operational transconductance amplifier (OTA) as the controller difference amplifier and by adding squelch switches [17]. The addition of squelch switches increase the update speed by disconnecting the control loop during memory cell update. The OTA for the control loop is shown in Figure 8. For effective operation, it is desirable for cascaded controller OTA to offer:

- High gain, in-order to effectively sense and amplify small voltage differences into large control signals.
- Simpler transistor matching to minimize offset voltages, since all transistors are of the same size.
- Low power operation.

The DC-gain of the amplifier $Av$ is given by:

$$Av \approx \left(\frac{gm_5}{gm_2}\right) \cdot \left(\frac{gm_{13} \cdot ro_{13} \cdot ro_{14}}{2}\right)$$

(26)

where $gm_i$ and $r_i$ are the transconductance and the channel conductance of transistor $Q_i$, respectively. The amplifier has a voltage gain ($Av$) of 10000. All the transistors in the amplifier have length and width of 18 µm and 9 µm respectively. Uniform transistor dimensions also offer an advantage of simpler transistor matching.

From Equation 27 we can use the dimensions for transistors $Q_1$ and $Q_4$ to control the maximum leakage compensation current allowable and in-turn loop speed of compensation. For our design, complementary gate switches have been dimensioned to ensure low leakage by making NMOS and PMOS body leakage currents almost equal in magnitude, since the effective leakage to the body is the difference between the NMOS and PMOS body leakage currents [15]. Additionally, since $|V_{DS}|_{max} = |V_{IN} - V_{OUT}|_{max} = \Delta V$, the channel leakage currents are also low. These aspects are advantageous since they reduce the compensation current required. The component dimensions are shown in Table I.

The memory cell’s equilibrium state is a state in which there are no changes in $V_D$ and $V_{OUT}$. This state is reached either
when the storage capacitors are empty or when there is perfect leakage cancellation \( I_L = I_C \). The memory cell controller’s output can be derived as follows:

\[
V_C = A_o(V_{OUT} - V_D - V_{OFF})
\]

where \( V_{OFF} \) is the OTA’s offset voltage. To function effectively, the OTA should have a high voltage gain and low input offset voltage, thus transistors must be well matched.

### B. Dynamic Comparator

Instead of using continuous time comparators, we use dynamic comparators. Dynamic comparators offer the following advantages:

- Lower power operation since the comparator is not active all the time.
- Higher power budget flexibility through duty cycling.
- Simpler interfacing with switched capacitor circuits.
- High immunity to noise.

The disadvantages of dynamic comparators are:

- They require an enable signal.
- Complex to model in simulators [31].

Dynamic comparators offer us the advantages of lowering power and having an architecture that is technology scaling friendly [32]. To minimize power consumption, we use the fully dynamic and mismatch robust Halonen architecture based dynamic comparators [33]. The use of a differential reference source offers an advantage of higher noise immunity. Figure 10 shows a schematic diagram of the dynamic comparator used. In Figure 10 \( V_{in}^{±} \), \( V_{ref}^{±} \) and \( V_{out}^{±} \) are the differential input, reference and output voltage signals respectively, while \( V_{latch} \) is the comparator enabling signal [33]. The dynamic comparator architectures offers highly flexible design choices [33]. The decision point of the dynamic comparator is determined by the currents \( I_{D3} \), \( I_{D4} \), \( I_{D5} \) and \( I_{D6} \) currents, which are in-turn controlled by the \( V_{in} \) and \( V_{ref} \) inputs. The comparator decision point is reached when \( I_{D3} + I_{D5} = I_{D4} + I_{D6} \). From Figure 10 we let \( W_4 = W_6 \) and \( W_5 = W_3 \), thus the input stage’s large signal behavior can be characterized by [33]:

\[
I_{D4} - I_{D3} = \beta_4 V_{in} \sqrt{\frac{2I_{D1}}{\beta_4} - V_{in}^2}
\]

\[
I_{D5} - I_{D6} = \beta_6 V_{ref} \sqrt{\frac{2I_{D2}}{\beta_6} - V_{ref}^2}
\]

where \( \beta_i = 1/2\mu_0 C_{ox} W_i / L_i \). \( V_{in} = V_{in}^{+} - V_{in}^{-} \) and \( V_{ref} \). The determination of the decision point should be done to allow the selection of reference voltages that are simpler to generate and work with. For practical reasons we require our reference voltage \( V_{ref} = V_{ref}^{+} - V_{ref}^{-} \) to be higher than our threshold voltage \( \Delta V \). This requirement simplifies the design of the reference voltage source. Equations 31 and 32 show the two scaling constants \( \tau \) and \( \gamma \) used for reference scaling.

\[
\tau = \frac{V_{in}}{V_{ref}}
\]

(31)

The variable \( \tau \) in Equation 31 allows us to scale the voltage to a value that can be practically supplied by a reference.

\[
\gamma = \frac{I_{D1}}{I_{D2}}
\]

(32)

Considering the comparator at decision point when \( I_{D3} + I_{D5} = I_{D4} + I_{D6} \), we can subtract Equations 29 and 30 to get:

\[
\beta_4 V_{in} \sqrt{\frac{2I_{D1}}{\beta_4} - V_{in}^2} = \beta_6 V_{ref} \sqrt{\frac{2I_{D2}}{\beta_6} - V_{ref}^2}
\]

We square Equation 33 and then divide it by \( V_{ref} I_{D2} \) to get Equation 34, which is in terms of \( \tau \) and \( \gamma \) to get the design equations for the decision point [33]:

\[
2\gamma \tau^2 I_{D2} \frac{W_4}{L_4} - \frac{1}{2} \mu_0 C_{ox} r^4 V_{ref}^2 \left( \frac{W_4}{L_4} \right)^2 = 2\gamma I_{D2} \frac{W_6}{L_6} - \frac{1}{2} \mu_0 C_{ox} V_{ref}^2 \left( \frac{W_6}{L_6} \right)^2
\]

(34)

We chose to have a \( V_{ref} \) that is about \( \tau \) times the level crossing voltage \( \Delta V (\tau = 100 \text{ and } \gamma = 0.1) \). The transistor dimensions of the comparator are given in Table IV.

### C. Finite State Machine and Data Path

The ADC’s operation is driven by a small finite state machine and data path (FSMD) shown in Figure 11. The operational state of the FSMD at any given time is determined by a reset signal (S-RESET) and three events whose occurrence

<table>
<thead>
<tr>
<th>Controller bridge dimensions</th>
<th>Length</th>
<th>Size (( \mu m ))</th>
<th>Width</th>
<th>Size (( \mu m ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1, L2</td>
<td>40</td>
<td>W1, W2</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td>L3, L4</td>
<td>40</td>
<td>W3, W4</td>
<td>0.5</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE I: Component dimensions for controller bridge.**

<table>
<thead>
<tr>
<th>Dynamic Comparator dimensions</th>
<th>Length</th>
<th>Size (( \mu m ))</th>
<th>Width</th>
<th>Size (( \mu m ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1, L3, L4</td>
<td>1</td>
<td>W1, W3, W4</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>L2, L5, L6</td>
<td>1</td>
<td>W2, W5, W6</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>L7, L8</td>
<td>0.5</td>
<td>W7, W8</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>L9, L10</td>
<td>0.5</td>
<td>W9, W10</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>L11, L12</td>
<td>0.5</td>
<td>W11, W12</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE II: Component dimensions for the dynamic comparator.**
rate depends on the input signal. The S-RESET signal is activated to initialize the state machine. The three events are categorized as two analogue front-end events (A-events) and timer generated events (T-events). The A-events are generated as follows:

- If the input of the difference amplifier DCU in Figure 2 is above the $\Delta V$ threshold, an increase event (A-EVENT-INC) is triggered.
- If the input of the difference amplifier DCD is above threshold, a decrement event (A-EVENT-DEC) is generated. Please note that since the dynamic comparators only sense one type of event, they are connected in Figure 2, such that a A-EVENT-DEC event occurs when the difference between the input and the memory cell signal goes below threshold.

If the signal's activity is below the $\Delta V$ threshold for a full timer period, a timer overflow event (T-EVENT-OVF) is generated. The finite state machine interprets both the A-events and the T-events and generates the control signals for the ADC. The state machine has only six states, which are: INIT, IDLE, A-DEC, A-INC, T-OVF, and DOUT. After applying the reset (S-RESET) signal, the state machine is initialized, the memory cell is updated with the input signal. The timer is reset and starts running, and the ADC goes into the IDLE state in which it waits for events. It stays in the IDLE state, until it receives an event.

If the input signal has no activity, eventually the timer will overflow, generating a T-EVENT-OVF event, which causes the ADC to go into the T-OVF state. In this state the timer overflows flag is set, the timer is reset which generates a D-HANDLE event.

If the input signal is increasing such that the output of the DCU differential amplifier in Figure 2 crosses the threshold voltage, the comparators trigger an A-EVENT-INC, which causes the ADC to enter the A-INC state, where it updates the analogue memory cell with the current signal value, captures the timer value and resets the timer and sets the signal increase flag which, generates a D-HANDLE event.

Likewise, if the input signal is decreasing the threshold crossing triggers an A-EVENT-DEC, which causes the ADC to enter the A-DEC state where it updates the analogue memory cell with the current signal value, captures the timer value and resets the timer and sets the signal decrease flag which generates a D-HANDLE event.

The D-HANDLE event causes the state machine to enter the DOUT state. In the DOUT state we appropriately encode the data depending on the event flag and then latch it using the DRY signal see Figure 2. The output data is composed of the timer value and a two bit flag indicating the event type. For overflows, the timer value is redundant, such that only the flag and count of overflows is necessary.

IV. Measurement Results

We implemented our proposed ADC architecture and fabricated a chip on the EM Microelectronic 0.35 $\mu$m CMOS technology process. The control logic was implemented on a Xilinx Spartan 3 FPGA, which allowed flexibility in analogue block characterization. A photo of the chip fabricated is shown in Figure 12. The proposed ADC occupies an area of $147\times253 \, \mu$m$^2$.

Fig. 11: Asynchronous ADC state machine.

Fig. 12: Pseudo asynchronous ADC chip micrograph. The ADC module has a size of $253 \times 147 \, \mu$m$^2$ on a 0.35 $\mu$m CMOS process; marked by a black rectangle.

A. ADC Performance Characteristics

Our target application is a low power, battery operated implantable ECG recorder, with a power supply voltage of 2.4 V. All measurements presented herein are done at a supply voltage of 2.4 V, unless specified otherwise. However, the fabricated ADC has been verified to work from 1.8 V to 2.4 V. The ADC front-end has an input frequency range between 0.05 Hz and 1 kHz with an ENOB of up to 8 bits and a signal to noise dynamic range SNDR of up to 48 dB. The ADC's performance characteristics are summarized in Table III. The front-end can support variable $\Delta V$ resolution between 4 and 8 bits.
**TABLE III: ADC characteristics.**

<table>
<thead>
<tr>
<th>Target application</th>
<th>ECG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>1.8 V to 2.4 V</td>
</tr>
<tr>
<td>ENOB</td>
<td>6 to 8 bits</td>
</tr>
<tr>
<td>ΔV Resolution</td>
<td>37 dB</td>
</tr>
<tr>
<td>SNDR</td>
<td>0.6 µW to 2.0 µW*</td>
</tr>
</tbody>
</table>

- The 1 MHz clock is for measurement purposes only, for ECG signals a clock rate of 32 768 Hz is sufficient.

# - Power consumption of 0.6 µW is achieved at a supply voltage of 1.8 V, while the power consumption of 2 µW is at 1 MHz clock frequency at supply voltage of 2.4 V.

B. Signal Accuracy

The dynamic range of the ADC was measured for a 1.0 V peak to peak input signal at various frequencies. We used cubic splines for reconstruction before applying the fast Fourier transform (FFT). Figure 13 shows the power spectrum diagram of the ADC at its maximum input frequency of 1 kHz, while Figure 14 shows the signal to noise dynamic range (SNDR) of the ADC front-end at various input signal frequencies and ΔV step size corresponding to resolution N. There is a lower SNDR for very low frequencies, caused the degradation in performance due to the limited memory cell hold time according to Equation 25. We also observe as expected, a drop in SNDR as the frequency is increased. According to Equation 20 we should expect an increase in time quantization associated errors (εVn) as the input frequency is increased. For these measurements the clock frequency was adjusted as the input signal frequency is increased as required by the Bernstein criterion in Figure 4. We also measured the dynamic performance of the ADC at different input levels. Figure 15 shows the SNDR against the input level in dB of the full scale input. We observed a drop in performance at low input signal levels. This is expected since there are fewer samples to reconstruct the data from. Asynchronous ADCs are known to have power consumption that is highly dependent on the input signal frequency. We carried out power measurements for our ADC front-end and its individual blocks, namely the memory cell and the dynamic comparator at different input frequencies. Figure 16 shows the power consumption in nW of the dynamic comparator, the memory cell and ADC front-end. The variation of power consumption of the ADC front-end due to the change in the power consumption of the dynamic comparators as the signal activity changes and clock rate is varied see Figure 4.

C. ECG Signal Measurement

To verify the functionality of the ADC for our intended application, we captured an ECG signal with our ADC front-end prototype. The signal is acquired with a clinical use certified G-Tech USB amplifier and stored on a PC for repeatability. From PC signal is converted back to analogue domain by a National Instruments signal converter box and fed to our ADC. Figure 17 shows the signal flow diagram.

Figure 18 shows the performance of our ADC front-end on a real ECG signal. For ECG signal acquisition with a timer clock rate of 32 768 Hz, the ADC front-end consumes only 0.6 µW at a supply voltage of 1.8 V and 1.7 µW at 2.4 V.
Fig. 16: Asynchronous ADC power consumption at supply voltage 2.4 V and $\Delta V$ resolution corresponding to 8 bits at various input signal frequencies. Input signal frequency is from 0.05 Hz to 1000 Hz. The scan frequency for each corresponding input signal frequency is: 0.05 Hz: 32 kHz, 100 Hz: 96 kHz, 200 Hz: 192 kHz, 300 Hz: 288 kHz, 400 Hz: 384 kHz, 500 Hz: 480 kHz, 600 Hz: 576 kHz, 700 Hz: 672 kHz, 800 Hz: 768 kHz, 900 Hz: 864 kHz, 1 kHz: 960 kHz.

D. Memory Cell Performance

The hold time of the memory cell has already been identified as an important performance measure at low frequencies. Figure 19 shows the hold times of the memory cell at different resolutions and input voltage signal levels. Figure 19 shows that there is a drop in hold time across input signal range. This reduction is due to a combination of factors, amongst them: increased leakages of capacitors and switches and OTA gain fluctuation due to the high input signal level. As expected, the memory cell has longer hold times at low resolutions. The equation is also the step size of the ADC is set 8 bits resolution step size, the impact of this decrease in hold time on the SNR is offset by the increase in sample density at the higher $\Delta V$ step resolution.

V. DISCUSSION

We have presented an architecture for a pseudo asynchronous ADC. The ADC architecture replaces the DAC with an analogue memory cell. The architecture also replaces continuous time comparators with more energy efficient and technology scaling friendlier dynamic comparators. The prototype chip fabricated covers a signal bandwidth of 0.05 Hz to 1 kHz. The ADC front-end is specifically designed for an implantable ECG signal acquisition system, where there are severe energy and space restrictions. In our envisioned applications there is a need to reduce both energy and memory to reduce the overall device volume. Asynchronous ADCs are very attractive when it comes to reducing both energy and the amount of data generated [2]. For a comparison of ECG data rates between level crossing ADCs and equidistant sampling ADCs, see [2]. Even though our architecture introduces overflow events these events, occur in bursts, in regions of low signal activity for ECG signals [36]. Therefore, they are simply counted into one counter value, hence there is little to no overhead.

A. Comparison with Other Works

In Table IV we have compared our ADC front-end to other low power asynchronous level crossing ADC designs. We have also introduced a figure-of-merit (FOM) given in Equation 35. The FOM takes into account four very common design requirements namely the power in $\mu$W, chip area in mm$^2$, $f_{Nyq}$ which is the Nyquist sampling frequency for the ADC input bandwidth and the ENOB. The equation is also the Walden FOM multiplied by the chip area.

$$FOM = \frac{\text{Power} \cdot \text{Area}}{f_{Nyq} \cdot 2^{\text{ENOB}}}. \quad (35)$$

We also consider whether a particular design’s specification is suitable for the purposes of ECG signal acquisition. This is an important attribute since our work is targeting ECG signals, additionally this introduces the very low frequency operation...
TABLE IV: Comparisons with other asynchronous level crossing ADCs designed for ECG signals (our work has off the chip logic).

(a) Chip includes a signal amplification front-end.
(b) Chip has additional hardware for adaptive resolution.
(c) This chip has for four channels including front-end amplifiers. Area given is for the ADC only per channel.
(d) Lowest power performance also includes a QRS peak detector.
(e) Lowest power performance is achieved at 1.8 V supply voltage.
(f) Lower cutoff bandwidth not specified but an ADC with the same specification was published by the authors used for ECG in [35].
(g) The reconstruction method has not been stated. However, from the figures in the publication, it looks like zero order hold reconstruction.

(*) The main limitation is the lower cut off bandwidth requirements.

<table>
<thead>
<tr>
<th>References</th>
<th>[3]</th>
<th>[34]</th>
<th>[4]</th>
<th>[10]</th>
<th>[2]</th>
<th>[5]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (μm)</td>
<td>0.13</td>
<td>0.18</td>
<td>0.35</td>
<td>0.5</td>
<td>0.18</td>
<td>0.13</td>
</tr>
<tr>
<td>Power supply (V)</td>
<td>0.8</td>
<td>1.0</td>
<td>0.7</td>
<td>5.3</td>
<td>1.8</td>
<td>0.3</td>
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<tr>
<td>Power (μW)</td>
<td>3-9</td>
<td>8.49(\text{a})</td>
<td>25(\text{b})</td>
<td>120(\text{c})</td>
<td>0.31-0.582</td>
<td>0.22(\text{d})</td>
</tr>
<tr>
<td>ENOB (bits)</td>
<td>8</td>
<td>8</td>
<td>8.4</td>
<td>5</td>
<td>6</td>
<td>4.4</td>
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<tr>
<td>Bandwidth (Hz)</td>
<td>20-20k</td>
<td>0.06-950</td>
<td>1(\text{f})</td>
<td>0.2k-20k</td>
<td>5-5k</td>
<td>0.05-1k</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>47.54</td>
<td>46.4-50.2</td>
<td>43.2-52.2</td>
<td>31</td>
<td>40-49</td>
<td>28.3</td>
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<tr>
<td>Area (mm(^2))</td>
<td>0.36</td>
<td>0.49</td>
<td>0.96</td>
<td>0.06(\text{e})</td>
<td>0.045</td>
<td>0.36(\text{d})</td>
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<td>DAC</td>
<td>5(\text{th}) order interpolation</td>
<td>6(\text{th}) order interpolation</td>
<td>Not stated(\text{g})</td>
<td>3(\text{rd}) – 6(\text{th}) order interpolation</td>
<td>Not stated(\text{g})</td>
</tr>
<tr>
<td>FOM</td>
<td>1.05c-07</td>
<td>8.55c-06</td>
<td>3.55c-05</td>
<td>5.63c-06</td>
<td>2.18c-08</td>
<td>1.889c-06</td>
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<tr>
<td>ECG Acquisition</td>
<td>No(\text{a})</td>
<td>Yes</td>
<td>Yes(\text{a})</td>
<td>No(\text{a})</td>
<td>No(\text{a})</td>
<td>Yes</td>
</tr>
</tbody>
</table>

B. Possible Improvements

The use of analogue memory cells opens room for possible improvements on the asynchronous ADC designs as the design of analogue memory cells improve. The memory cell architecture can be improved to have lower power consumption and longer hold times. Moreover, there are memory cell architectures that exist with ultra low power consumption as low as 10 nW with long hold times in the range of minutes at 12 bits of resolution [17]. However, these designs in their current form have a drawback of having update times, as long as 10 ms, which is too high for our application [17]. Improvements of these architectures to lower update times would enable lowering power and improvements in performance of the ADC architecture presented. It is also important to note that as technology scales downwards the memory cell architecture may also need to be changed to ensure that the area is kept minimal [17]. There is also room for improvement on the dynamic comparators in terms of linearity which would improve the SNDR performance of the ADC. Furthermore, performance of the system may be improved by adding a difference and buffering stage before the comparators. This would improve performance by reducing comparator kickback effect at the expense of increased power consumption.

VI. CONCLUSIONS

We have designed and fabricated the proposed ADC in 0.35 μm CMOS technology. The design occupies a small chip area and consumes low power. A major goal in the design of implantable continuous signal acquisition systems, such as the latest leadless pacemakers, is to minimize the overall size of the system. This is achieved by minimizing the chip size, energy consumption and memory size of the system. It is well known that level crossing ADCs generate fewer samples than their Nyquist counter parts. On top of this inherent sample reduction it also generates sparse time information that can further be compressed and encoded with low computational effort and can be represented by an even smaller number of bits [36]. Besides low power and small chip area, the proposed architecture features dynamic comparators which make the proposed asynchronous level crossing ADC simpler to interface with synchronous system blocks such, as dedicated processing cores or micro-controllers.

REFERENCES
